HIGHLY INTEGRATED SINGLE PACKAGE MONOLITHIC VCO/ UP-CONVERTER FOR DIGITAL MICROWAVE RADIO SYSTEMS

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ABSTRACT

It is shown that with state-of-the-art microwave CAD and enhanced active and passive modelling, the concept of a highly integrated low cost macro-function inside a single package can be successfully extended up to microwave frequencies. Simulated and measured results are presented on three integrated VCO/ frequency up-converters designed and fabricated at C-, X- and Ku-band frequencies.

INTRODUCTION

Frequency up-conversion for Digital Microwave Radio Systems is usually based upon the following three microwave circuits:

(a) a dual output Voltage Controlled Oscillator (VCO) with a Dielectric Resonator (DR) allowing a good phase noise

(b) a diode or FET based Mixer to convert an IF frequency of less than 2 GHz into the microwave range

(c) a low level amplifier providing the required gain at the output

One of the two VCO's outputs has to be fed into an external Phase Lock Loop (PLL) which applies a voltage to the VCO's varactor in order to adjust its oscillation frequency.

This paper demonstrates that all these three microwave circuits (except the Dielectric Resonator coupled to an external 50 Ohms line) can be monolithically integrated into a single micro-package, combining GaAs and Silicon technologies. Making use of state-of-the-art CAD software and extensive modelling, one can come up with a first pass design allowing not only a better scientific understanding but which is also the key to an economically interesting fast time to market component. Figure (1) presents the synoptic block diagram for all C, X and Ku frequency bands and figure (2) exhibits a photograph of the C-band prototype.

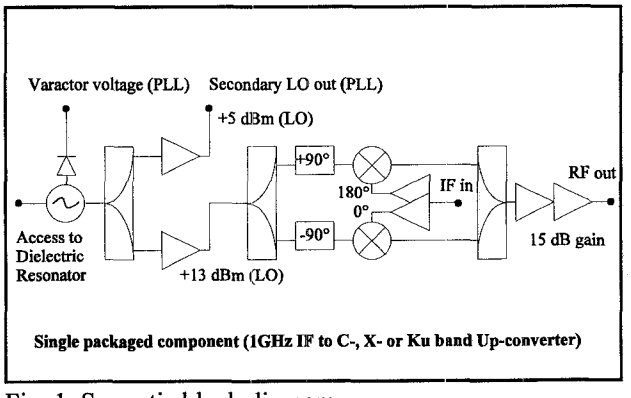

Fig. 1: Synoptic block diagram

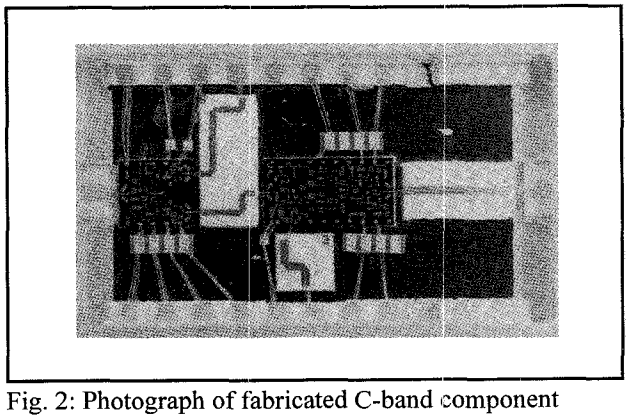

Fig. 2: Photograph of fabricated C-band component

Chosen technology and circuit topology

For C, X & Ku band operation, TRIQUINT SEMI-CONDUCTOR's 0.5µm GaAs MESFET MMIC process was chosen for the VCO and MIXER/ RF-AMPLIFIER chips. The micro-package is a KYOCERA custom design developed for multi I/O microwave components.

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The VCO is linked to an independent Silicon VARACTOR chip for phase noise purposes. A good phase noise is also achieved through a Dielectric Resonator external to the package. Two buffer FETs allow a saturated and less temperature dependent VCO output power.

The MIXER is single balanced for 45dB guaranteed LO rejection and uses two cold resistive FET's for high linearity, so that the IF input power can be as high as possible. The necessary 180° for the 750-1750 MHz IF are generated by a single active FET. Approximately 15dB of RF gain are provided by a two stage amplifier implemented on the same mixer chip. A very thorough modeling of active and passive components allows a purely passive 180° LO phase shifter without any electrical tuning requirements for LO rejection.

Overview of Simulated Characteristics, VCO and MIXER design guidelines

All simulations are based on the HP-EESOF ACADEMY 3.5 CAD package, associated with LIBRA (harmonic balance) and MW-SPICE (time domain analysis including transmission lines).

(1) GaAs VCO CHIP + Silicon VARACTOR CHIP + external Dielectric Resonator:

- Small signal "negative resistance" input reflection coefficient S11, including process sensitivity analysis at the desired frequency

- Verification of start-up conditions using time domain analysis as shown in figure (3)

- Determination of steady state conditions (stabilized oscillation frequency, oscillation output power, degree of saturation, generated harmonics)

- Frequency variation slope of varactor in MHz/V (for PLL) versus technology process variations

(2) GaAs single balanced LO REJECTION up-converting MIXER/AMPLIFIER CHIP:

- Conversion gain flatness, Spurious at the RF output, Third order intercept point of the cascaded mixer and two stage amplifier

- LO rejection versus technology process variations (passive LO phase shifter)

Packaging

Although no three dimensional electromagnetic simulator has been used to optimize the complete integration of all chips and substrates into the micro-package, all RF feed-throughs of the package and all bond wires are taken into account for the electrical performance. In this case, we have verified that the ceramic RF feed-throughs can be simulated on a linear simulator by using a simple micostrip and stripline description. The micro-package was defined with a cut-off frequency high enough for our application and thus exhibits more than 50dB of isolation up to Ku-band.

Modelling of active devices and passive elements

The key FET (6x50µm) was characterized using DC pulsed I/V measurements [1] and multi-bias on-wafer S-parameters in order to derive non linear TAJIMA type and splined models for different bias points. The varactor chips were soldered onto an alumina substrate, connected with a bond wire to a transmission line and then measured using a CASCADE MICROTECH probe. The Dielectric Resonator was characterized inside its cavity with a special test fixture.

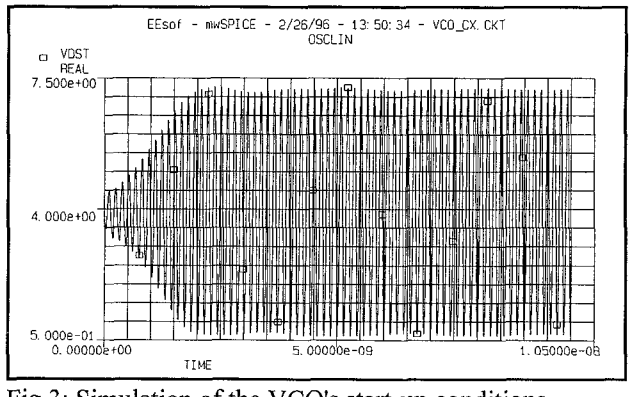
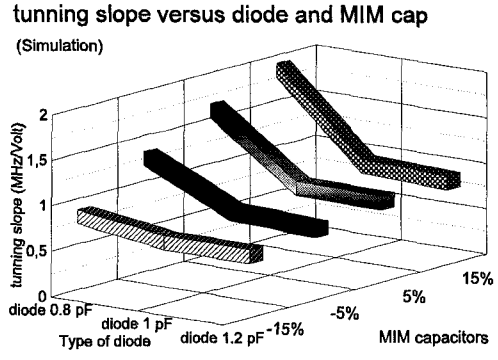
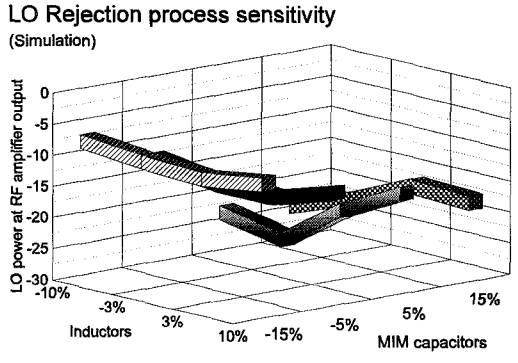


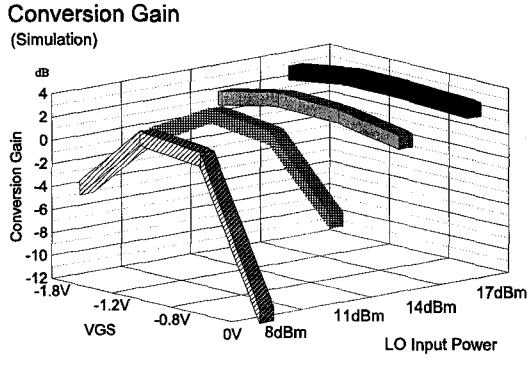
Fig.3: Simulation of the VCO's start-up conditions

Yield analysis simulations

A very robust design for the majority of all sub-circuits and a thorough yield analysis of most critical parameters are the key to a first pass design and product. Figure (4) presents the impacts of simulated process variations on some main performances of the packaged C-band VCO/ Up-converter. Much more parameters than the ones presented on the view charts must be accounted for during the simulations, especially those of the active devices.







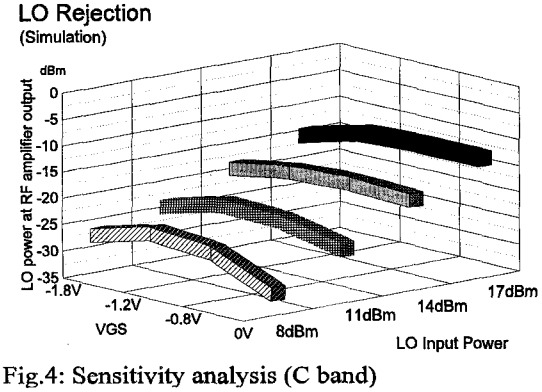


Fig.4: Sensitivity analysis (C band)

MEASURED PERFORMANCE

The packaged VCO/ Up-converters typically exhibit better than 0dB conversion gain with 1dBpp flatness over an IF frequency range of 750-1750 MHz. They are quite linear with a third order intercept point higher than +15dBm at the IF input and guarantee less than -15dBm LO power at the RF output in C, X & Ku band. Internally, more than 12dBm LO power are generated with a phase noise of 100dBc/Hz @100KHz (free running). A coupled LO output of 5dBm is available for an external PLL.

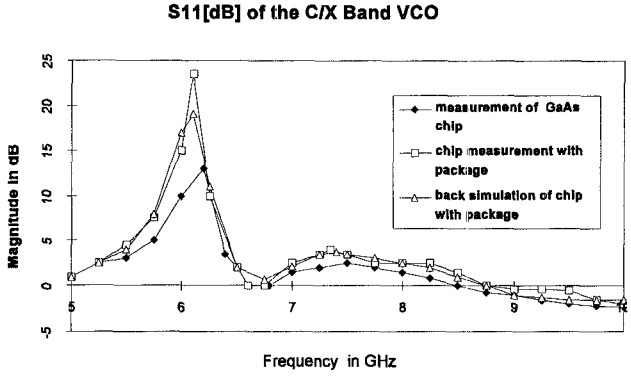


Fig.5: Measured and simulated S11 of packaged VCO

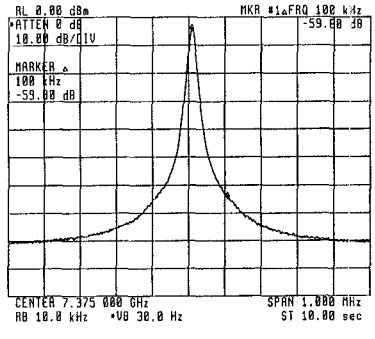


Fig.6: Measured phase noise (C band)

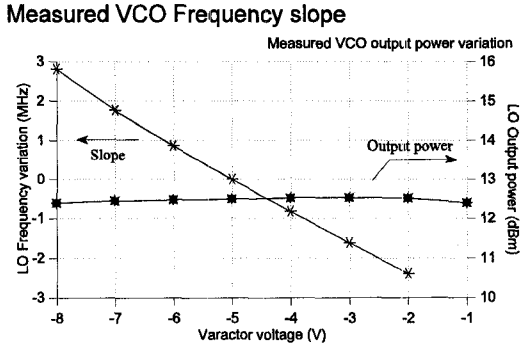


Fig.7: Measured slope and LO output power (C band)

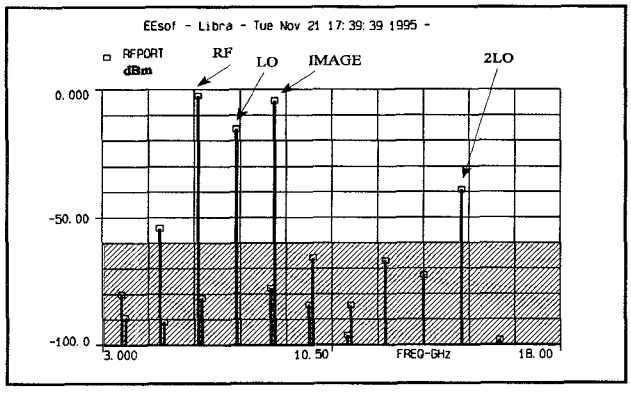


Fig.8: Simulated output spectrum for P(IF)= -5dBm

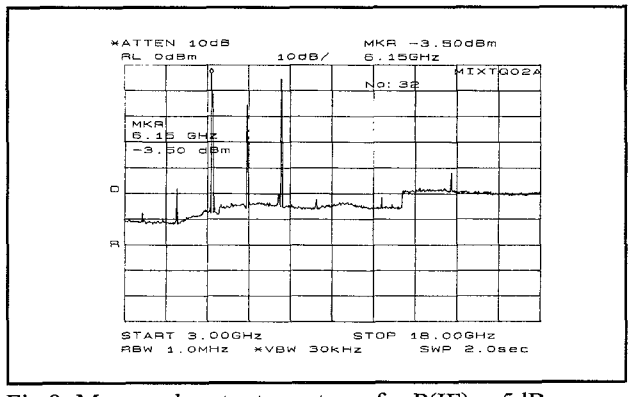


Fig.9: Measured output spectrum for P(IF)= -5dBm

CONCLUSION

Our aim was to exhibit a concrete example where taking into account the packaged environment since the beginning of the individual MMIC designs can come up with a first pass "macro"-component of high interest for an industrial application. More and more designers have to think about final production yield and choose the right topology from the beginning. An important factor of a first pass success is the investment in enhanced modelling: today's software packages are able to treat thousands of elements (LINES, BENDS, TEES, black box elements, etc.), including very sophisticated non linear descriptions of active devices like splined or TAJIMA like pulsed I/V curve models which users can implement themselves.

REFERENCES

[1] B. Rattay, M. Hübner, J.P. Teyssier, R. Quéré, "Accurate Hemt modeling for non-linear simulation", in *Proceedings of the 22nd European Microwave Conference*, pp. 1201-1205

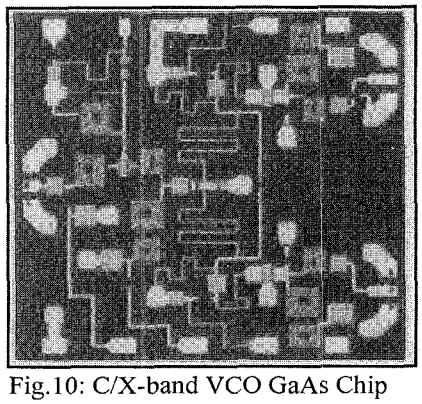


Fig.10: C/X-band VCO GaAs Chip

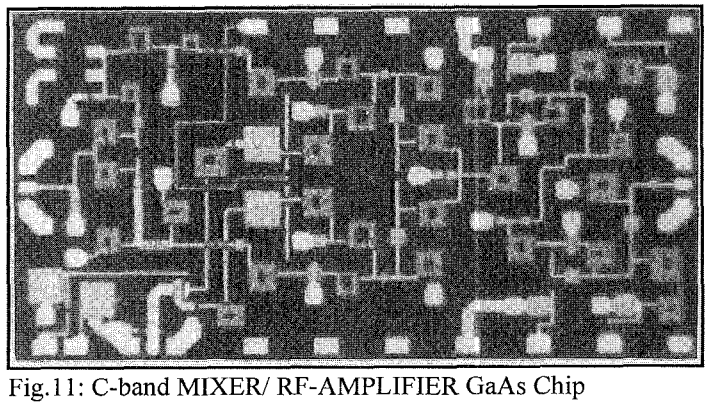


Fig.11: C-band MIXER/ RF-AMPLIFIER GaAs Chip

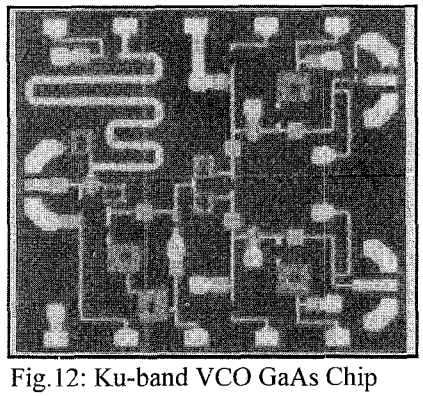


Fig.12: Ku-band VCO GaAs Chip

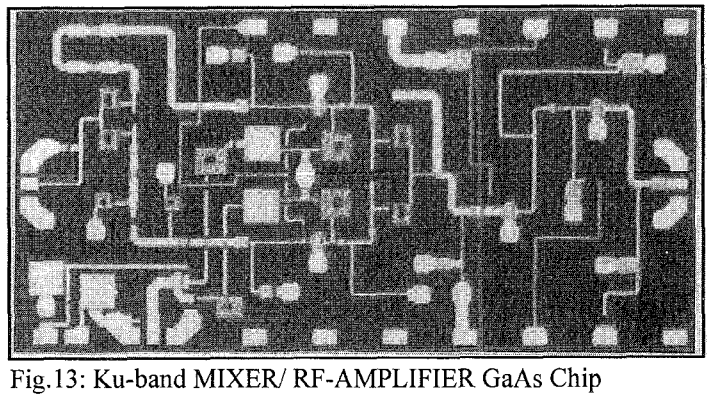


Fig.13: Ku-band MIXER/ RF-AMPLIFIER GaAs Chip